WHAT IS CLAIMED IS:

- 1. A radio frequency (RF) down-convertor with reduced local oscillator leakage, for demodulating an input signal *x*(*t*), comprising:
- a synthesizer for generating mixing signals ϕ_1 and ϕ_2 which vary irregularly over time, where ϕ_1 * ϕ_2 has significant power at the frequency of a local oscillator signal being emulated, and neither ϕ_1 nor ϕ_2 has significant power at the frequency of said local oscillator signal being emulated;
- a first mixer coupled to said synthesizer for mixing said input signal x(t) with said mixing signal φ_1 to generate an output signal x(t) φ_1 ; and
- a second mixer coupled to said synthesizer and to the output of said first mixer for mixing said signal x(t) φ_1 with said mixing signal φ_2 to generate an output signal x(t) φ_1 φ_2 .
- 2. The radio frequency (RF) down-convertor of claim 1 wherein said synthesizer further comprises:
- a synthesizer for generating mixing signals φ_1 and φ_2 , where $\varphi_1 * \varphi_1 * \varphi_2$ does not have a significant amount of power within the bandwidth of said input signal x(t) at baseband.
- 3. The radio frequency (RF) down-convertor of claim 2, further comprising: a DC offset correction circuit.
- 4. The radio frequency (RF) down-convertor of claim 3, wherein said DC offset correction circuit comprises:
- a DC source having a DC output; and
- a summer for adding said DC output to an output of one of said mixers.
- 5. The radio frequency (RF) down-convertor of claim 2, further comprising: a closed loop error correction circuit.
- 6. The radio frequency (RF) down-convertor of claim 5, wherein said closed loop error correction circuit further comprises:
- an error level measurement circuit and
- a time-varying signal modification circuit for modifying a parameter of one of said mixing signals ϕ_1 and ϕ_2 to minimize said error level.



- 7. The radio frequency (RF) down-convertor of claim 6, wherein said error level measurement circuit comprises a power measurement.
- 8. The radio frequency (RF) down-convertor of claim 6, wherein said error level measurement circuit comprises a voltage measurement.
- 9. The radio frequency (RF) down-convertor of claim 6, wherein said error level measurement circuit comprises a current measurement.
- 10. The radio frequency (RF) down-convertor of claim 6, wherein said modified parameter is the phase delay of one of said mixing signals ϕ_1 and ϕ_2 .
- 11. The radio frequency (RF) down-convertor of claim 6, wherein said modified parameter is the fall or rise time of one of said mixing signals ϕ_1 and ϕ_2 .
- 12. The radio frequency (RF) down-convertor of claim 6, wherein said modified parameter includes both the phase delay and the fall or rise time of one of said mixing signals φ_1 and φ_2 .
- 13. The radio frequency (RF) down-convertor of claim 2 wherein said synthesizer further comprises:
- a synthesizer for generating mixing signals ϕ_1 and ϕ_2 , where said mixing signals ϕ_1 and ϕ_2 can change with time in order to reduce errors.
- 14. The radio frequency (RF) down-convertor of claim 1, further comprising: a filter for removing unwanted signal components from said x(t) ϕ_1 signal.
- 15. The radio frequency (RF) down-convertor of claim 1, wherein said mixing signals ϕ_1 and ϕ_2 are random.
- 16. The radio frequency (RF) down-convertor of claim 1, wherein said mixing signals ϕ_1 and ϕ_2 are pseudo-random.
- 17. The radio frequency (RF) down-convertor of claim 1, wherein said mixing signals ϕ_1 and ϕ_2 are irregular.



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18. The radio frequency (RF) down-convertor of claim 1, wherein said mixing signals ϕ_1 and ϕ_2 are digital waveforms.

- 19. The radio frequency (RF) down-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are square waveforms.
- 20. The radio frequency (RF) down-convertor of claim 1, further comprising: a local oscillator coupled to said synthesizer for providing a signal having a frequency that is an integral multiple of the desired mixing frequency.
- 21. A method of demodulating a radio frequency (RF) signal x(t) with reduced local oscillator leakage comprising the steps of:

generating mixing signals ϕ_1 and ϕ_2 which vary irregularly over time, where ϕ_1 and $*\phi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither ϕ_1 nor ϕ_2 has significant power at the frequency of said local oscillator signal being emulated;

mixing said input signal x(t) with said mixing signal φ_1 to generate an output signal x(t) φ_1 ; and

mixing said signal x(t) φ_1 with said mixing signal φ_2 to generate an output signal x(t) φ_1 φ_2 .

- 22. An integrated circuit comprising the radio frequency (RF) down-converter of claim 1.
- The radio frequency (RF) down-converter of claim 1, where said synthesizer uses different patterns to generate signals φ_1 and φ_2 .
- 26. The radio frequency (RF) down-converter of claim 1, wherein said synthesizer uses a single time base to generate both mixing signals ϕ_1 and ϕ_2 .

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WHAT IS CLAIMED IS:

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- 1. A radio frequency (RF) down-convertor with reduced local oscillator leakage, for demodulating an input signal x(t), comprising:
- a synthesizer for generating mixing signals ϕ_1 and ϕ_2 which vary irregularly over time, where ϕ_1 ϕ_2 has significant power at the frequency of a local oscillator signal being emulated, and neither ϕ_1 nor ϕ_2 has significant power at the frequency of said local oscillator signal being emulated;
- a first mixer coupled to said synthesizer for mixing said input signal x(t) with said mixing signal φ_1 to generate an output signal x(t) φ_1 , and
- a second mixer coupled to said synthesizer and to the output of said first mixer for mixing said signal x(t) φ_1 with said mixing signal φ_2 to generate an output signal x(t) φ_1 φ_2 .
- The radio frequency (RF) down-convertor of claim 1 wherein said synthesizer further comprises:
- a synthesizer for generating mixing signals ϕ_1 and ϕ_2 , where $\phi_1 * \phi_2 * \phi_2$ does not have a significant amount of power within the bandwidth of said input signal x(t) at baseband.
- 3. The radio frequency (RF) down-convertor of claim 2, further comprising: a DC offset correction circuit.
- 4. The radio frequency (RF) down-convertor of claim 3, wherein said DC offset correction circuit comprises:
- a DC source having a DC output; and a summer for adding said DC output to an output of one of said mixers.
- 5. The radio frequency (RF) down-convertor of claim 2, further comprising: a closed loop error correction circuit.
- 6. The radio frequency (RF) down-convertor of claim 5, wherein said closed loop error correction circuit further comprises:

an error level measurement circuit and

a time-varying signal modification circuit for modifying a parameter of one of said mixing signals ϕ_1 and ϕ_2 to minimize said error level.

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- 7. The radio frequency (RF) down-convertor of claim 6, wherein said error level measurement circuit comprises a power measurement.
- 8. The radio frequency (RF) down-convertor of claim 6, wherein said error level measurement circuit comprises a voltage measurement.
- 9. The radio frequency (RF) down-convertor of claim 6, wherein said error level measurement circuit comprises a current measurement.
- 10. The radio frequency (RF) down-convertor of claim 6, wherein said modified parameter is the phase delay of one of said mixing signals φ_1 and φ_2 .
- 11. The radio frequency (RF) down-conventor of claim 6, wherein said modified parameter is the fall or rise time of one/of said mixing signals ϕ_1 and ϕ_2 .
- 12. The radio frequency (RF) down-convertor of claim 6, wherein said modified parameter includes both the phase delay and the fall or rise time of one of said mixing signals φ_1 and φ_2 .
- 13. The radio frequency (RF) down-convertor of claim 2 wherein said synthesizer further comprises:
 a synthesizer for generating mixing signals φ₁ and φ₂, where said mixing signals φ₁ and φ₂ can change with time in order to reduce errors.
- 14. The radio frequency (RF) down-convertor of claim 1, further comprising: a filter for removing unwanted signal components from said x(t) ϕ_1 signal.
- 15. The radio frequency (RF) down-convertor of claim 1, wherein said mixing signals ϕ_1 and ϕ_2 are random.
- 16. The radio frequency (RF) down-convertor of claim 1, wherein said mixing signals φ, and φ₂ are pseudo-random.
- 17. The radio frequency (RF) down-convertor of claim 1, wherein said mixing signals φ₁ and φ₂ are irregular.

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The radio frequency (RF) down-convertor of claim 1, wherein said mixing signals ϕ_1 and ϕ_2 are digital waveforms.

- The radio frequency (RF) down-convertor of claim 1, wherein said mixing signals φ₁ and φ₂ are square waveforms.
- 20. The radio frequency (RF) down-convertor of claim 1, further comprising: a local oscillator coupled to said synthesizer for providing a signal having a frequency that is an integral multiple of the desired mixing frequency.

21. The radio frequency (RF) down-convertor of claim 1, wherein said synthesizer uses a single time base to generate both mixing signals ϕ_1 and ϕ_2 .

- 722. The radio frequency (RF) down-convertor of claim 1, where said synthesizer uses different patterns to generate signals φ_1 and φ_2 .
- 23. A method of demodulating a radio frequency (RF) signal x(t) with reduced local oscillator leakage comprising the steps of:

generating mixing signals φ_1 and φ_2 which vary irregularly over time, where $\varphi_1 = \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;

mixing said input signal x(t) with said mixing signal φ_1 to generate an output signal $x(t) \varphi_1$; and

mixing said signal x(t) ϕ_1 with said mixing signal ϕ_2 to generate an output signal x(t) ϕ_1 ϕ_2

An integrated circuit comprising the radio frequency (RF) down-convertor of any one of claims 1 - 22.

25. A computer readable memory medium, storing computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio frequency (RF) down-convertor of any one of claims 1 - 22.

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A computer data signal embodied in a carrier wave, said computer data signal comprising computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio frequency (RF) down-convertor of any one of claims 1 - 22.

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